

Docket No. 020417

Serial No. 10/765,766

REMARKS/ARGUMENTS

This Amendment is responsive to the Office Action mailed February 9, 2005. Applicant has amended claims 1, 14, 19, 20, 31 and 32, and added new claims 43-45. Claims 1-45 are now pending in the present application.

Objection to Drawings

In the Office Action, the Examiner objected to the drawings, stating that "all signals directly involve element 112 of figure 2 appears to have nothing to do with rest of the circuit." Applicant is confused by the Examiner's remarks. Consequently, the basis of the Examiner's objection to the drawings is unclear.

As described in Applicant's disclosure, "FIG. 2 illustrates a series of waveforms and associated spectra for a clock circuit that utilizes additional circuitry to select a rising or falling edge of the input clock to trigger the rising edge of the output clock." Accordingly, FIG. 2 shows clock timing waveforms for an ideal input clock, an ideal output clock, and an M:N divided output clock.

Element 112 is a reference clock and is described with respect to FIGS. 5 and 6 in conjunction with an exemplary embodiment in which a clock circuit selects a rising or falling edge of an input clock signal to trigger both the rising and falling edges of an output clock signal. Reference clock 112 does not appear in FIG. 2. The relationship between reference clock 112 of FIGS. 5 and 6 and the timing diagram of FIG. 2, as apparently perceived by the Examiner, is unclear to Applicant.

Applicant respectfully requests that the Examiner provide additional details concerning the objection to the drawings, so that Applicant may formulate an appropriate response. Applicant does not request that the objection to the drawings be held in abeyance. Rather, Applicant respectfully traverses the objection to the drawings for lack of details sufficient to support such an objection.

Allowable Subject Matter

In the Office Action, the Examiner allowed claims 1-13. In addition, the Examiner objected to claims 15-18, 21-30 and 33-42 as being dependent upon a rejected base claim, but indicated that such claims would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

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**Claim Rejection Under 35 U.S.C. § 102**

In the Office Action, the Examiner rejected claims 14, 19, 20, 31 and 32 under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,667,638 to Kramer et al. Applicant respectfully traverses the rejection, at least to the extent the rejection may be considered applicable to claims 14, 19, 20, 31, and 32, as amended. Kramer et al. fails to disclose each and every feature of the claimed invention, as required by 35 U.S.C. 102(e), and provides no teaching that would have suggested the desirability of modification to include such features.

Applicant has amended claims 14, 19, and 31 to improve the clarity of those claims, for reasons unrelated to patentability. Claims 14, 19, and 31 now specify generation of an output clock signal such that a rising edge of selected cycles of the output clock signal is based on a rising edge of an input clock signal, a rising edge of other selected cycles of the output clock signal is based on a falling edge of the input clock signal, a falling edge of selected cycles of the output clock signal is based on a rising edge of the input clock signal, and a falling edge of other selected cycles of the output clock signal is based on a falling edge of the input clock signal.

Hence, according to claims 14, 19, and 31, the rising edge of the output clock signal is based on either the rising edge or the falling edge of the input clock signal. Likewise, the falling edge of the output clock signal is based on either the rising edge or the falling edge of the input clock signal. Original claims 14, 19 and 31 already included such requirements, although the amendments may make them even more clear.

In either case, Kramer et al. fails to disclose or suggest such features. Kramer et al. describes a frequency divider that utilizes an asynchronous slip request signal to provide an output clock signal according to an odd-numbered divide ratio. The slip request signal activates a slip signal so that the transition of a divided signal is skipped.

Kramer et al. does not disclose the selection of a rising edge of an output clock signal based on either a rising edge or a falling edge of an input clock signal. Moreover, Kramer et al. fails to suggest the selection of a falling edge of an output clock signal based on either a rising edge or a falling edge of the input clock signal. Indeed, the Kramer et al. reference does not even mention a falling edge, whether for an input clock signal or output clock signal.

In support of the rejection, the Examiner pointed to the circuit depicted in FIG. 1 of Kramer et al. The Examiner stated that the circuit receives an input clock signal with a rising

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edge and a falling edge, noting that all clock signals have rising and falling edges. According to the Examiner, control circuit 170 generates an output clock signal and selects a rising edge based on a rising edge or falling edge of the input clock signal, and selects a falling edge of the output clock signal based on a rising edge or falling edge of the input clock signal.

As discussed above, Kramer et al. does not make any mention of a falling edge of the input clock signal, much less selection of a rising edge of the output clock signal based on the falling edge of the input clock signal. If the Examiner's interpretation of the original claims was that the requirements could be satisfied by selecting the rising and falling edges of the output clock signal based on the rising and falling edges, respectively, of the input clock signal, such interpretation would be improper.

First, the original claims required selection of each of the rising and falling edges of the output clock signal based on either the rising or falling edge of the input clock signal. The amendments to claims 14, 19 and 31 should make these differences even more clear. Second, it is unclear whether there is any relationship between the falling edges of the input and output clock signal in the Kramer et al. circuit, much less a relationship between the rising edges and falling edges of the output clock signal.

Thus, Kramer et al. fails to disclose each and every limitation set forth in claims 14, 19, 20, 31, and 32. For at least these reasons, Kramer et al. does not support a *prima facie* case of anticipation of such claims. Applicant respectfully request withdrawal of the rejection under section 102(e).

New Claims:

Applicant has added claims 43-45 to the pending application. No new matter as been added by the new claims.

Claim 43 specifies that the control circuit of claim 1 is configured to select a rising edge of some cycles of the output clock signal based on a rising edge of the input clock signal, and a rising edge of some other cycles of the output clock signal based on a falling edge of the input clock signal, and to select a falling edge of some cycles of the output clock signal based on a rising edge of the input clock signal, and a falling edge of some other cycles of the output clock signal based on a falling edge of the input clock signal.

Claims 44 and 45 specify that the control circuit is configured to generate selected cycles of the output clock signal with a rising edge based on a rising edge of the

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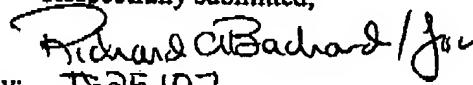
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input clock signal, and selected cycles of the output clock signal with a rising edge of the output clock signal based on a falling edge of the input clock.

### CONCLUSION

All claims in this application are in condition for allowance. Applicant respectfully requests reconsideration and prompt allowance of all pending claims. Please charge any additional fees or credit any overpayment to deposit account number 17-0026. The Examiner is invited to telephone the below-signed attorney to discuss this application.

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Respectfully submitted,  
  
By: DC 26,107  
Donald C. Kordich  
Attorney for Applicant  
Registration No. 38,213

QUALCOMM Incorporated  
5775 Morehouse Drive  
San Diego, California 92121-2779  
Telephone: (858) 658-5928  
Facsimile: (858) 658-2502